12bit SAR AD converter IC

MM3802A12WBE
Datasheet

FUNCTION

12-bit Successive Approximation Type Analog to Digital Converter IC

FEATURES

- High sampling rate 200Ksps
- Full differential Analog input
- 3～5V Digital interface adaptive
- Low power, Automatic shutdown

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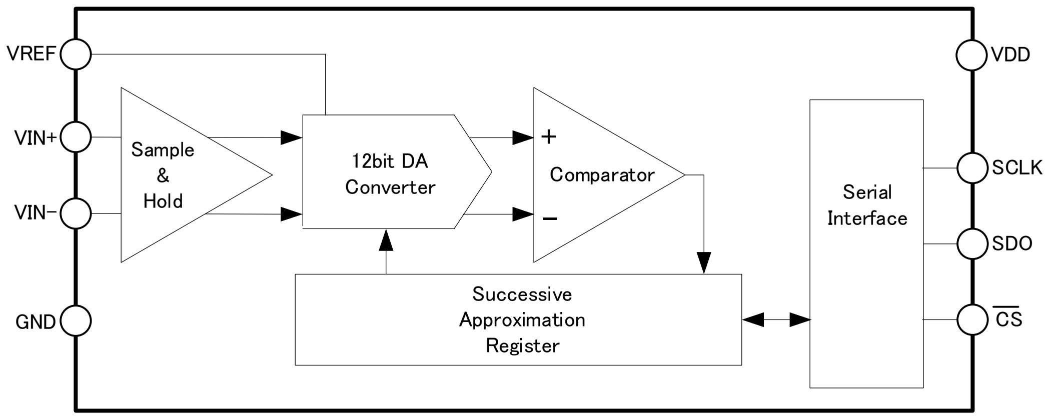
BLOCK DIAGRAM



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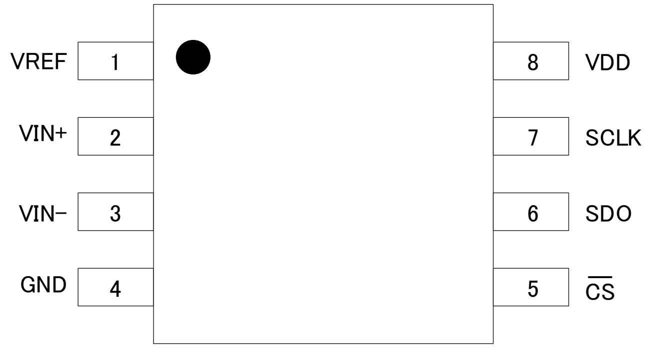
PIN CONFIGURATION



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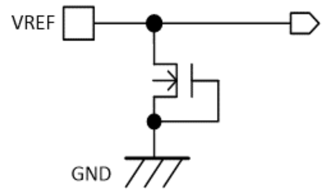
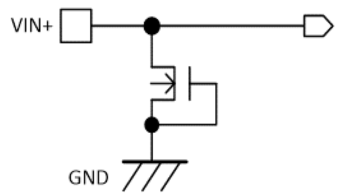
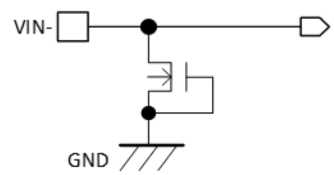
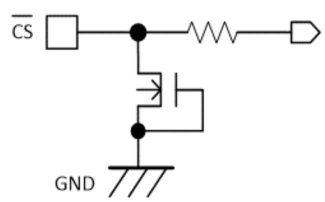
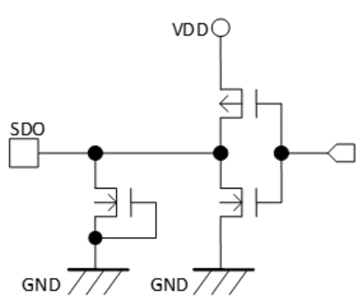
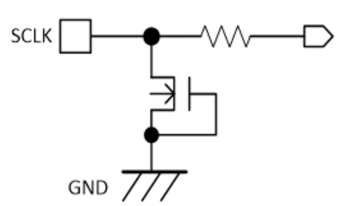
TERMINAL EXPLANATIONS

PIN No.	SYMBOL	TYPE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
1	VREF	Input		Reference voltage input
2	VIN+	Input		Plus analog input
3	VIN-	Input		Minus analog input
4	GND	-	-	Ground
5	$\overline{CS}$	Input		Chip select input $\overline{CS}$ / ADC 'Low' / Active 'High' / Power down
6	SDO	Output		Serial communication data output
7	SCLK	Input		Serial communication clock input

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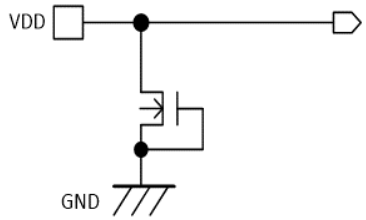
8	VDD	-		Power supply

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ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	VDD	-0.3	6.0	V
Input voltage	(note[1])	GND-0.3	VDD+0.3	V
Storage temperature	Tstg	-40	125	deg.C
Power dissipation	Pd	-	180	mW

note[1]: VIN+, VIN-, VREF, $\overline{CS}$, SDO, SCLK

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Operating ambient temperature	Top	-40	85	deg.C
VDD operating voltage	VDDop	4.75	5.25	V

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ELECTRICAL CHARACTERISTICS

(unless otherwise specified, Ta=25deg.C, VDD=5V, Vref=2.5V, Sampling rate(fsample)=200Ksps, fclk=16 × fsample, VIN-=2.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD supply current						
Supply current (Active)	Isu	fclk=3.2MHz fsample=200Ksps	-	460	800	μA
		fclk=3.2MHz (note[2]) fsample=12.5Ksps	-	40	80	μA
		fclk=200kHz fsample=12.5Ksps	-	330	600	μA
Supply current (Power down)	Iprdn	$\overline{CS}$='High'	-	0	3	μA
		SCLK='Low'				
Analog Input						
Full-scale input range	FSR	(VIN+) - (VIN-)	-Vref	-	Vref	V
Input capacitance (note[3])	Cina		-	15	-	pF
Input eakage current	Iina		-1.0	0.0	1.0	μA

note[2]: fclk=3.2MHz, $\overline{CS}$='High' for 241 clock cycles out of every 256.
note[3]: Specified by design.

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(unless otherwise specified.,Ta=25deg.C, VDD=5V, Vref=2.5V, Sampling rate(fsample)=200Ksps, fclk=16×fsample, VIN-=2.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltage input						
Reference input voltage	Vref		0.1	-	2.5	V
Current drain1	Iref	fsample=200Ksps At code 000h	-	20	100	μA
Current drain2	Iref	$\overline{CS}$='High'	-	0	3	μA
Resolution						
Resolution	Reso		-	-	12	bits
No missing codes	Nmc		11	-	-	bits
Sampling dynamics						
Data rate	fsample		-	-	200	Ksps
Clock frequency	f_{clk}		0.032	-	3.2	MHz
DC accuracy						
Integral nonlinearity	INL		-2	-	2	LSB
Differential nonlinearity	DNL		-2	-	2	LSB
Input offset error	Vof		-6	-	6	LSB
Input offset thermal drift (note[3])	dVof/dt		-	±0.04	-	LSB/deg.C
Gain error	Gerr		-4	-	4	LSB
Gain error thermal drift (note[3])	Gerr/dt		-	±0.02	-	LSB/deg.C
Common mode rejection ratio	CMRR		-	72	-	dB
Power supply rejection ratio	PSRR		-	72	-	dB

note[3] : Specified by design.
LSB means Least Significant bit. When Vref is 2.5V, 1 LSB is 1.22mV.

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AC accuracy						
Total harmonic distortion	THD	-0.5dB[full scale] at 1kHz	-	-83	-	dB
		-0.5dB[full scale] at 5kHz	-	-81	-	dB
Signal to noise + distortion	SINAD	-0.5dB[full scale] at 1kHz	-	71	-	dB
Spurious free dynamic range	SFDR	-0.5dB[full scale] at 1kHz	-	86	-	dB
Digital input						
High level input voltage	Vih		2.4	-	VDD+0.3	V
Low level input voltage	Vil		-0.3	-	0.8	V
Digital output						
High level output voltage	Voh	Ioh=-250μA	3.5	-	-	V
Low level output voltage	Vol	Iol=+250μA	-	-	0.4	V

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TIMING CHARACTERISTICS

(unless otherwise specified., Ta=25deg.C, VDD=5V, Vref=2.5V, Sampling rate(fsample)=200Ksps, fclk=16 × fsample, VIN-=2.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock period	t_{clk}		312.5	-	-	ns
Clock duty	Duty		40	-	60	%
Acquisition time	t_{acq}		1.5	-	2	Clk Cycles
Conversion time	t_{conv}		-	12	-	Clk Cycles
$\overline{CS}$ 'High' time	t_{cs}		1	-	-	Clk Cycles
Setup time from $\overline{CS}$ falling to SCLK falling	t_{clkd1}		-	-	0	ns
Setup time from $\overline{CS}$ falling to SCLK rising	t_{clkd2}		30	-	-	ns
SDO tri-state delay time	t_{sdoz}		5	15	50	ns
SDO output delay time	t_{sdod}		5	15	50	ns
SDO fall time	t_{sdof}	Cload=100pF	-	40	120	ns
SDO rise time	t_{sdor}	Cload=100pF	-	50	120	ns

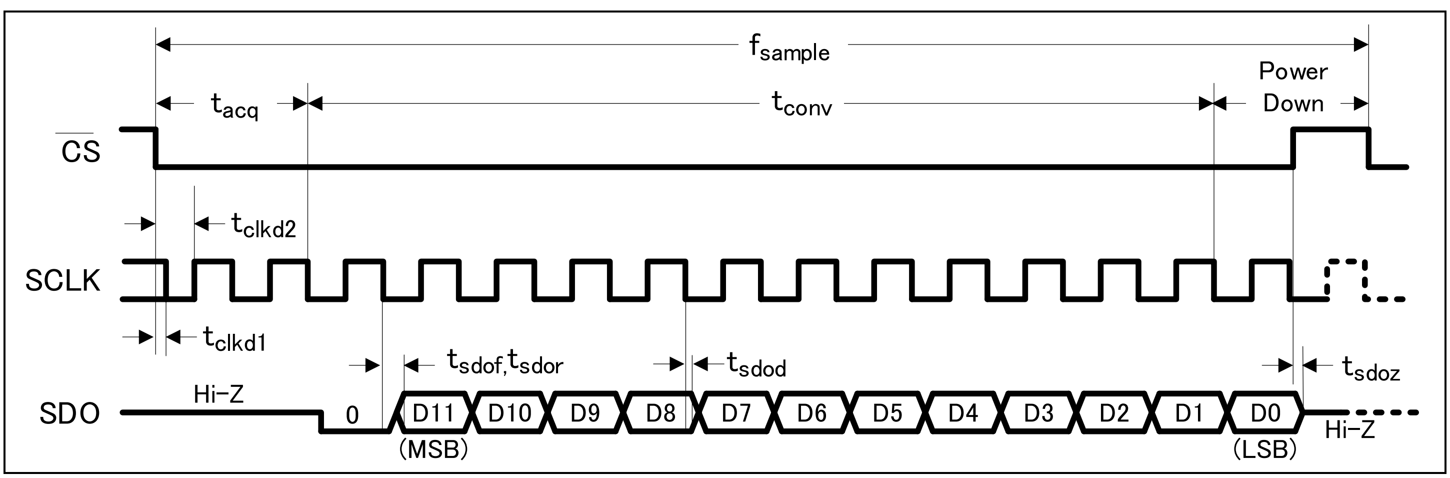

Fig. 1 Basic Timing Diagram

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DETAILED DESCRIPTION

DESCRIPTION OF ANALOG TO DIGTAL CONVERSION

The MM3802 is a successive approximation type of A/D converter IC, which can convert 12-bit data at 200 Ksps. It can collect data through the communication with external digital host via SPI compatible serial interface. As shown in Fig. 2, MM3802 starts sampling at a falling $\overline{CS}$ signal and ends it at the next falling edge of the clock. At the same time, internal conversion starts. Then, SDO is enabled and outputs 'Low' for one clock period. For the next 12 clocks period, SDO outputs the conversion result in most significant bit first order.
As shown in Fig. 3, after the least significant bit (D0) is output, subsequent clocks repeat the data output in least significant bit first order. When the most significant bit (D11) is output again, the subsequent data is output in this bit (D11). Since MM3802 ends the internal conversion after tconv, it enters the power down mode to reduce power consumption. When $\overline{CS}$ is 'High' under any conditions, SDO enters the tri-state mode. Then, MM3802 shifts to the power-down mode and returns to the initial state.

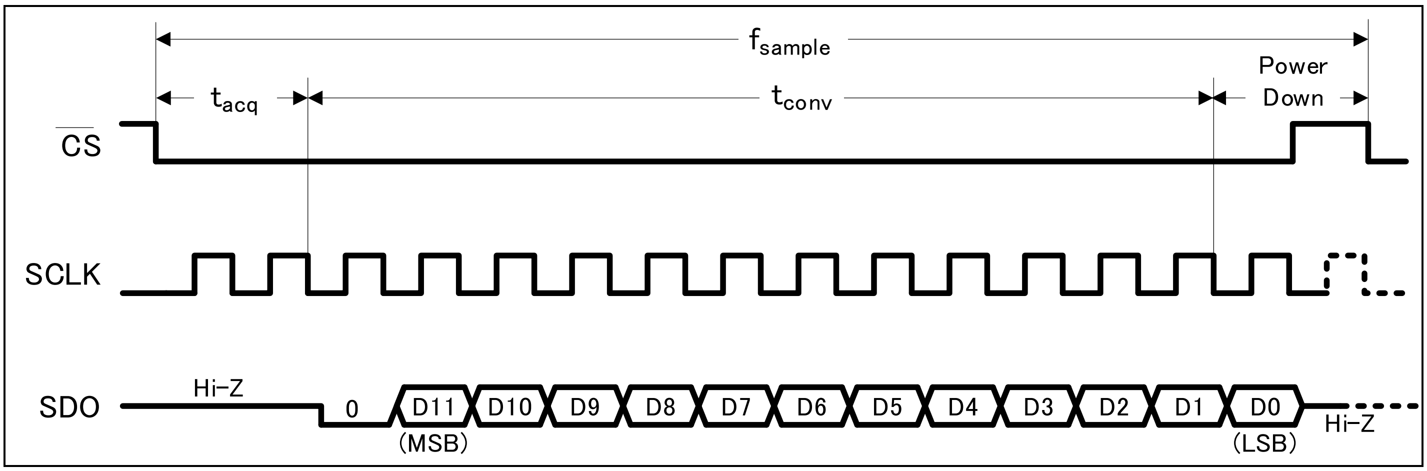

Fig. 2 Timing Diagram 1

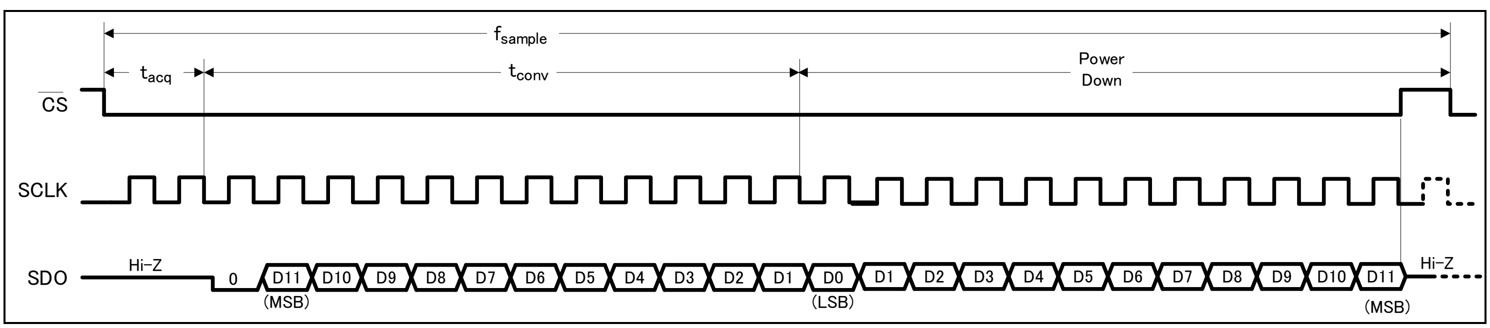

Fig. 3 Timing Diagram 2

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POWER DISSIPATION

The power consumption of MM3802 is directly proportional to the conversion rate at the constant clock rate. To minimize the power consumption, it is recommended to optimize the sampling rate for the system by adjusting the time of $\overline{CS}$='High' while the clock remains 3.2MHz. MM3802 enters the power down mode when the conversion is completed or $\overline{CS}$ is 'High'.

ANALOG INPUT

The analog input corresponds to fully differential input.
Since 15pF-input capacitance needs to be charged within acquisition time for both VIN+ and VIN-, output impedance from the external circuit to the IC should be appropriately set to reduce settling errors.

DATA FORMAT

The output data is in Binary Two's Complement format. Table 1 shows analog input voltage and ideal output codes.

Table 1 Ideal input voltages vs output codes

State	Differential Input Voltage (VIN+)−(VIN−)	Output Code		
		BIN	HEX	DEC
+Full scale	Vref−1LSB	0111 1111 1111	7FF	2047
Middle scale	0V	0000 0000 0000	000	0
Middlescale−1LSB	0V−1LSB	1111 1111 1111	FFF	−1
−Full scale	−Vref	1000 0000 0000	800	−2048

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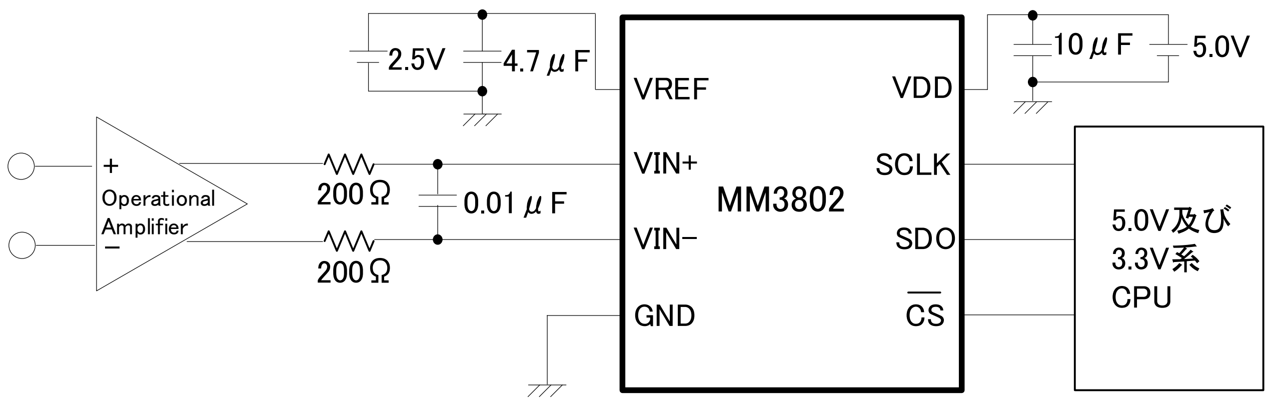
TYPICAL APPLICATION CIRCUIT



APPLICATION HINTS

- The VDD must be connected in close proximity 1μF to 10μF ceramic capacitor have effect that the system stability about voltage ripple or imported noise.
- The VREF must be connected in close proximity 1μF to 10μF ceramic capacitor.
- Strengthen the VDD and the GND wiring enough to cause the noise and the unstable operation when impedance is high.
- It is recommended to verify the external filter constant for VIN + and VIN - with the actual device.

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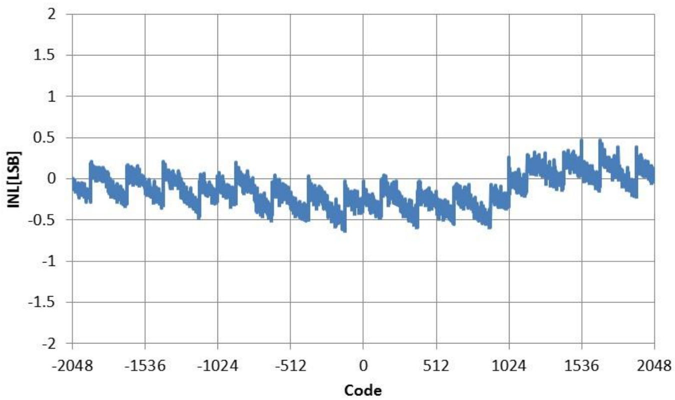
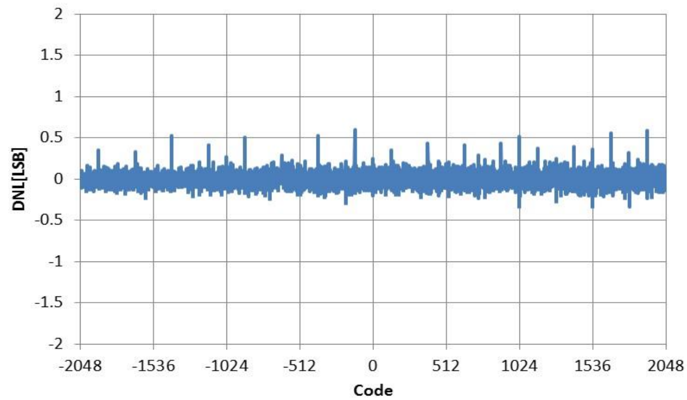
TYPICAL PERFORMANCE CHARACTERISTICS

(unless otherwise specified. Ta=25deg.C, VDD=5V, Vref=2.5V, Sampling rate(fsample)=200Ksps, fclk=16 × fsample, VIN-=2.5V)

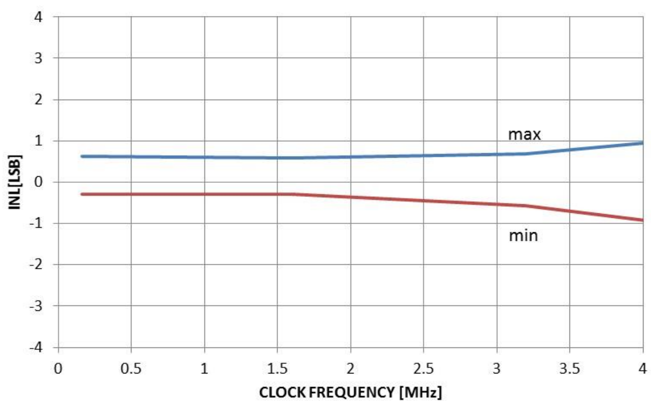
・ Integral nonlinearity (fclk=3.2MHz)



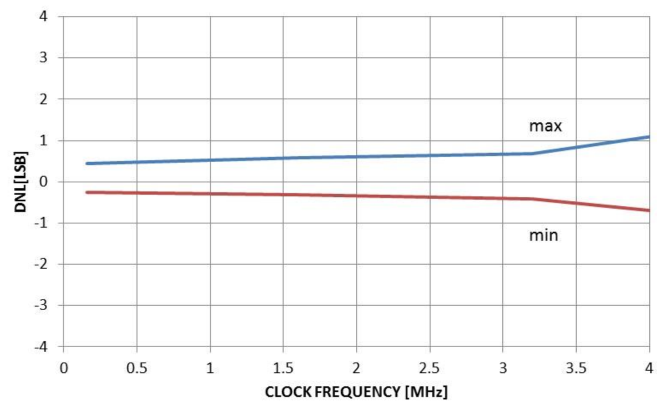
・ Differential nonlinearity (fclk=3.2MHz)



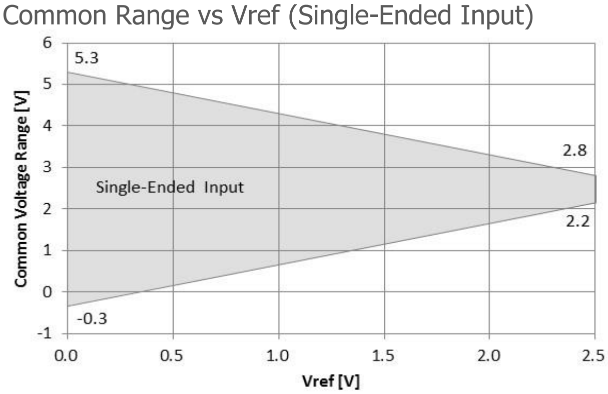
・ Integral nonlinearity vs CLK Frequency



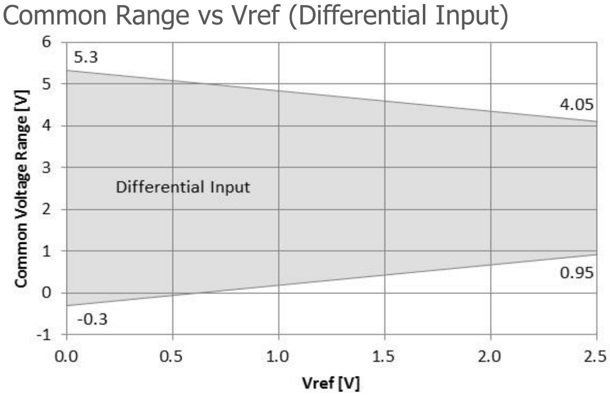
・ Differential nonlinearity vs CLK Frequency



・ Common Range vs Vref (Single-Ended Input)



・ Common Range vs Vref (Differential Input)



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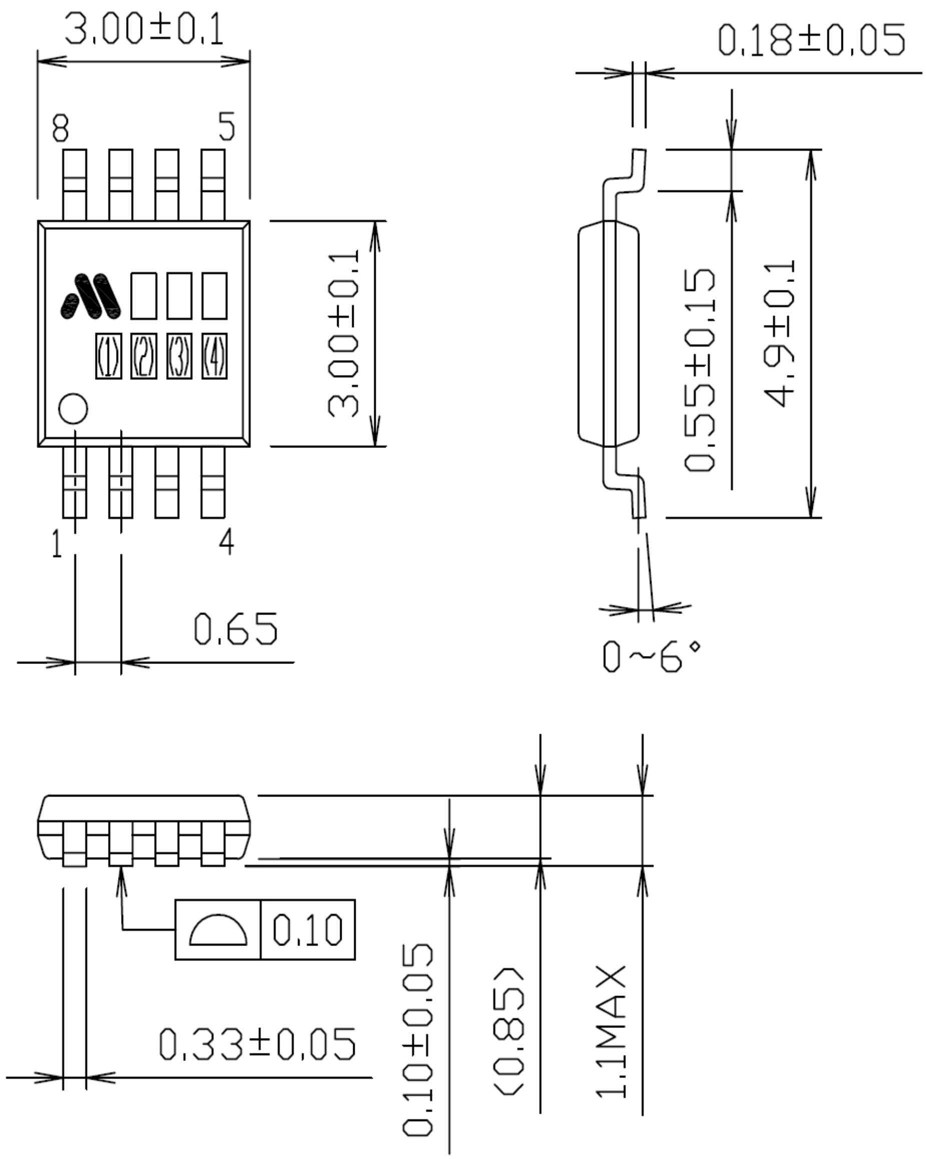
DIMENSIONS

PACKAGE : VSOP-8E

UNIT	mm



No.W08-VSOP8E-0001

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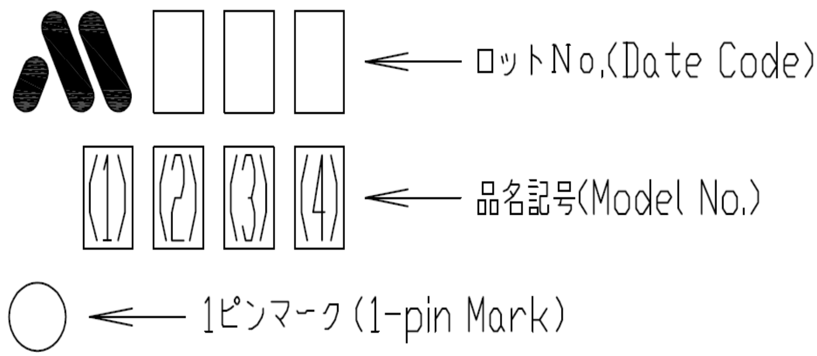
MARKING CONTENTS



Model name	Model No.			
	(1)	(2)	(3)	(4)
M M 3 8 0 2 A 1 2 W B E	2	A	1	2

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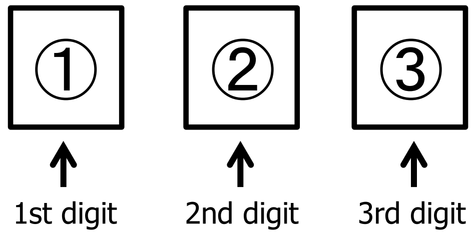
How to identify 3 characteristic lot numbers



1. The 1st digit (①) shows the last digit of a production year (western calendar).
2. The 2nd (②) and 3rd (③) digit show a production week of mass production.

【How to indicate a production year】

The 1st digit (①)	
the last digit of a production year	mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

The 2nd and 3rd digit (②③)			
production week	mark	production week	mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53

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- Before using this product, please evaluate and confirm the actual application with this product mounted and embedded.
- To investigate the influence by applied transient load or external noise, It is necessary to evaluate and confirm them with mounting this product to the actual application.
- Any usage above the maximum rating may destroy this product or shorten the lifetime. Be sure to use this product under the maximum rating.
- If you continue to use this product highly-loaded (applying high temperature, large current or high voltage; or variation of temperature) even under the absolute maximum rating and even in the operating range, the reliability of this product may decrease significantly. Please design appropriate reliability in consideration of power dissipation and voltage corresponding to the temperature and designed lifetime after confirming our individual reliability documents (such as reliability test report or estimated failure rate). It is recommended that, before using this product, you appropriately derate the maximum power dissipation (typically, 80% or less of the maximum value) considering parameters including ambient temperature, input voltage, and output current.

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